	Application No.	Applicant(s)
Notice of Allowability	10/769,818	SUGIO, KENICHIRO
	Examiner	Art Unit
	Huan Hoang	2818
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to		
2. The allowed claim(s) is/are <u>1-5.</u>		
3. The drawings filed on 03 February 2004 are accepted by the Examiner.		
<ul> <li>4.</li></ul>		
Paper No./Mail Date  Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).		
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
<ul> <li>Attachment(s)</li> <li>1. ☑ Notice of References Cited (PTO-892)</li> <li>2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)</li> <li>3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 020304</li> <li>4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material</li> </ul>	6. ☐ Interview Summary Paper No./Mail Dat 8), 7. ☐ Examiner's Amendn	e

Art Unit: 2818

## **REASONS FOR ALLOWANCE**

1. The following is an examiner's statement of reasons for allowance:

Claims 1-5 recite a semiconductor integrated circuit.

The prior art does not teach the following:

the memory cell has a cutoff circuit that cuts off the other bit line to hold voltage thereof produced by pre-charging when the bit information held in the memory cell is read out.

a cutoff section that keeps connection between the bit line pair pre-charged to write new bit information in the memory cell and the output section cut off until next writing.

an equalizer that cuts the bit line pair pre-charged in the former readout in two consecutive cycles of readout for bit information held in the memory cells off from pre-charge potential supply ports and equalizes, in the next readout, respectively potentials held in the bit lines of the bit line pair by the cutoff.

Therefore, the application is in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Art Unit: 2818

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Mon-Fri 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Huan Hoang Primary Examiner Art Unit 2818

HH 12/27/04.